A Ferroelectric FET CAM-Based Time-Domain In-Memory Computing Macro with 550 ps Delay Steps in 28 nm CMOS

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Nonvolatile in-memory computing (nvIMC) integrates storage and computation to reduce costly data movement. While analog nvIMCs [1,2] support in-memory multiply-accumulate (MAC), they suffer from noise and large data converters. Time-domain nvIMC (TD-nvIMC) improves energy efficiency by encoding computation as cumulative delays of cascaded delay elements (DEs), modulated by activations (X_i) and stored weights ($W_{i,j}$) [3-4].

This work presents a reconfigurable TD-nvIMC macro fabricated in GlobalFoundries 28 nm CMOS, integrating a FeFET-based content-addressable memory (CAM), DE chain, and time-to-digital converter (TDC). The architecture, shown in **Fig. 1a**, uses complementary FeFET pairs in a C-AND array [5] to store binary $W_{i,j}$. Each CAM output drives a current-starved inverter with a parallel leaker NMOS, forming a DE stage where the delay is set by the FeFET threshold voltage and wordline (WL) voltage. The DE chain output is sampled by a TDC with tunable reference line, converting delays to digital outputs. Our proof-of-concept (PoC) macro includes a 3×3 CAM, 3-stage DE chain, 2-bit TDC, and I/O drivers, occupies 17.6×30.7 μm² (**Fig. 1b**) and is probed on-die.

Fig. 2 presents measured results for the fabricated macro. The XOR-based MAC operation (**Fig. 2a**) is performed by grounding the BL of the selected row, applying X_i to WL_i, and their complements to $\overline{WL_i}$. A match between the input and stored weight ($X_i = W_{i,j}$) creates a fast discharge path, resulting in low delay t_{dL}, while a mismatch leads to high delay t_{dH}. This operation is experimentally validated across all possible input combinations, achieving a measured delay step of ~1.3 ns. For the AND-based MAC (**Fig. 2b**), $\overline{WL}$ is held at 0 V, so a fast discharge path exists only when $W_{i,j}$= X_i=1, achieving a 550 ps step, nearly 2000× smaller than prior demonstrations [3,4].

Beyond MAC, the same macro directly executes in-memory Boolean logic operations on the stored FeFET states. The logic operation depends on the FeFET states in the participating columns. **Fig. 2c** shows multi-bit logic by sampling specific TDC thermometer outputs. An AND operation across *k* selected bits, out of *M* columns, is realized by sampling TDC_{Th}[M-k], which only triggers when all selected cells store '1'. Similarly, logic OR is performed by sampling TDC_{Th}[M], which responds if at least one selected cell is '1'.

In summary, this work demonstrates a reconfigurable FeFET-based TD-nvIMC macro that supports binary XOR and AND-based MAC operations and in-memory logic, achieving 550 ps step size, a measured throughput of 2 GOPS for this 3×3 PoC macro designed for functionality demonstration, and 1887 TOPS/W energy efficiency from a 0.85-V supply.

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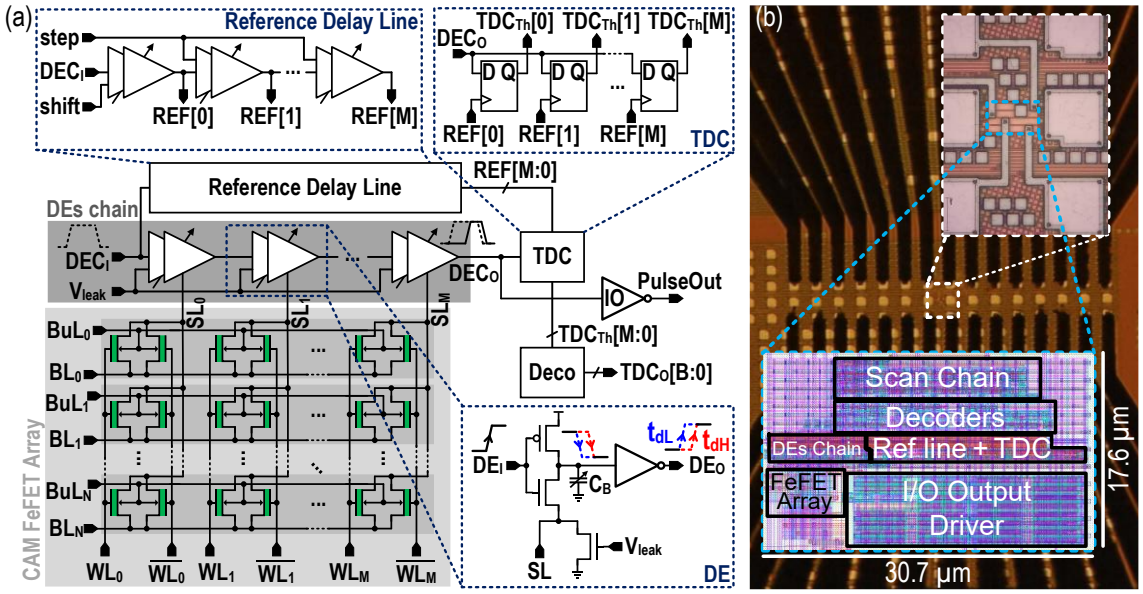
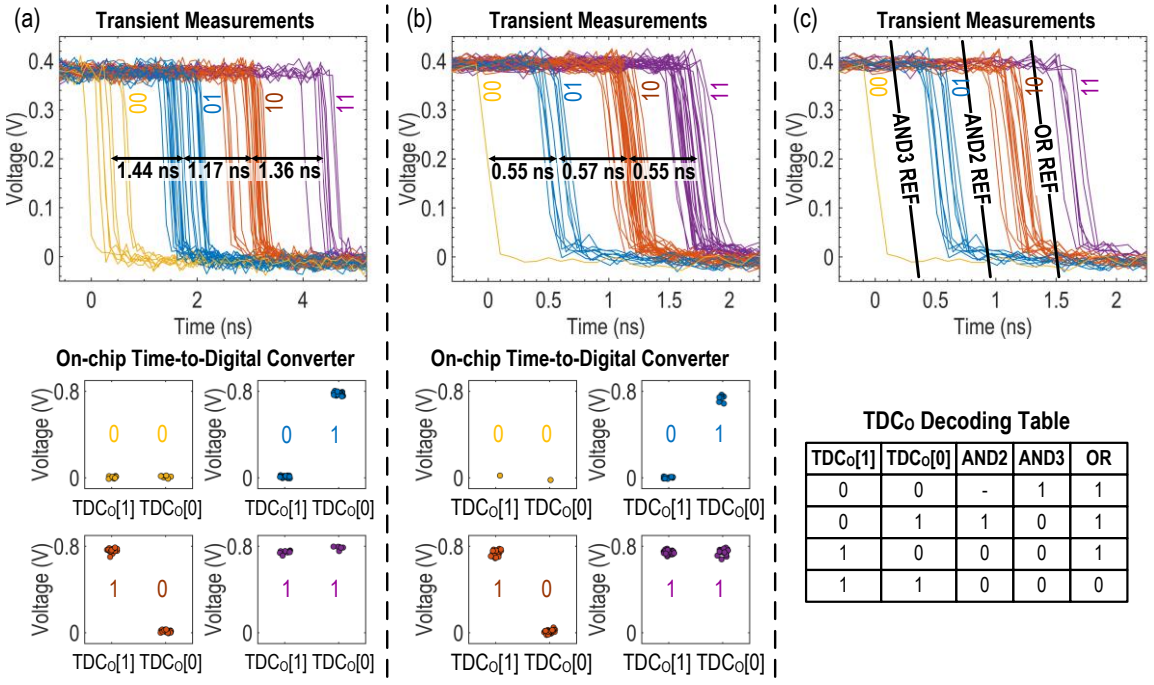


Fig. 1. (a) Proposed TD-nvIMC macro architecture composed of a DE chain with CSI whose tail is implemented by a CAM cell and a leaker driving an inverter, TDC with tunable reference delay line, and IO for observability. (b) Optical micrograph, on-die probing image, and layout.



TDCO[1]	TDCO[0]	AND2	AND3	OR
0	0	-	1	1
0	1	1	0	1
1	0	0	0	1
1	1	0	0	0

Fig. 2. (a) XOR-based MAC experimental results. TDC_O: 00 (+3), 01 (+1), 10 (-1), 11 (-3). (b) AND-based MAC experimental results. TDC_O: 00 (+3), 01 (+2), 10 (+1), 11 (0). (c) In-memory Boolean logic operations for two and three inputs experimental results and truth table.

References

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